M. Tech - *Signal Processing, Communication & Networks*
Department of Electrical Engineering
Indian Institute of Technology, Kanpur

Aravind Potluri

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Education & Relevant Courses

Master of Technology (SPCOM) - *Indian Institute of Technology Kanpur, Kanpur, CPI - 7.78* **2023 - 2025**

- Digital Communications and Networks, Mathematical Optimization, Introduction to Machine Learning, Data Structures & Algorithms

Bachelor of Technology (ECE) - *Indian Institute of Space Science and Technology, Trivandrum, CGPA - 7.01* **2019 - 2023**

- Basic Electrical and Electronics Engineering, Analog Circuits, Semiconductors Devices, Digital Circuits and VLSI, Instrumentation, Network Analysis, Computer Architecture, Computer Networks, Power Electronics, Advanced Sensors, Intro to MEMs, Basic Programming (c++), *Miscellaneous*: Principles of Management, Communication skills.

Intermediate (Maths, Physics & Chemistry) - *Ascent Junior College, Visakhapatnam , Percentage - 95.5%* **2016 - 2018**

Matriculation (Maths & Sciences) - *Visakha Valley School, Visakhapatnam, CGPA - 10* **2015 - 2016**

Work Experience

Flight Software Intern - *Agnikul Cosmos, Chennai* **Jan' 2023 - Jun' 2023**

- Implemented Time-Sensitive Networking (TSN 802.1) in the flight architecture to ensure low-latency, reliable communication, enhancing data control and system synchronization. And designed a robust network architecture integrating TSN, SPI, and UART (RS422/RS232) protocols for reliable and efficient in-flight communication.

Project Intern - *URSC:ISRO, Bangalore* **Jun' 2022 - Jul' 2022**

- Optimized CCMP and GCMP protocols to reduce time complexity, achieving a nearly tenfold boost in processing speed. These enhancements significantly improve the efficiency and reliability of space communication systems.

Research

Robust Techniques for Indoor Localization and Sensing - *Indian Institute of Technology Kanpur* **May' 2024 - May' 2025**

- *M.Tech Thesis* under the supervision of Dr. S. Swamy Peruru and Dr. Amitangshu Pal, focused on enhancing localization accuracy in non-line-of-sight (NLOS) and sparse access point environments through the utilization of IEEE 802.11ac/ax devices. The research also explores innovative sensing methodologies.

Position of Responsibilities

Chair Person - *IEEE EdSoc Chapter IIST* **Jun' 2022 - Aug' 2022**
General Secretary - *IEEE Student Branch IIST* **Aug' 2022 - Dec' 2022**
Teaching Assistant - *ESC201: INTRODUCTION TO ELECTRONICS Lab under Prof. K.S Venkatesh* **Jan' 2024 - May' 2024**
Teaching Assistant - *EE698K: PROGRAMMING FOR SIGNAL PROCESSING under Dr. Vipul Arora* **Aug' 2024 - Dec' 2024**

Skills

Programming Languages	C/C++, Bash, Python, VHDL/Verilog, Ada.
Software & Tools	LTSpice, KiCAD, ModelSim, Xilinx-Vivado, Git, LabVIEW, Yocto Project, Buildroot.
Technical Skills	Computer Architecture & Organization, FPGA Programming, ASIC Design, Embedded Systems, Machine Learning/AI, Kernel Programming, Version Control Systems.

Certifications

Verilog HDL | The Bits and Bytes of Computer Networking | Operating Systems and You
Open Source and the 5G Transition | Learn Linux Kernel Programming | Guide to Linux Kernel Development

Projects

Data Structures and Algorithms Python Library: [EE689 | LINK]

- Implemented a comprehensive DSA library, optimized for performance and usability as an educational tool for students.

Assessing the Vulnerability of CAR-PUFs Using SVM: [CS771 | LINK]

- Demonstrated security vulnerabilities of CAR-PUFs using minimal training data with mathematical modeling & SVM.

Backend Development for Navigation Correlator in IIST's NavIC Hardware: [SELF | LINK]

- Developed the backend for the Navigation Data Correlator tailored for IIST's NavIC hardware using UART and pandas.

Verilog based pipelined MIPS32 Implementation: [SELF | LINK]

- Developed a 32-bit MIPS32 pipelined processor with multi-instruction handling, validated by a detailed testbench.

Verilog based 64x64 Memory Module Design: [SELF | LINK]

- Designed a 64x64 memory module in Verilog with full read/write control, validated through a comprehensive testbench.